REMARKS

Claims 1-54 are pending in the present application. In the office action mailed October 13, 2004 (the "Office Action"), claims 1, 2, 4-11, 13-20, 22-29, 31-38, and 40-54 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,625,585 to Ahn *et al.* (the "Ahn patent"). Claims 3, 12, 21, 30, and 39 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Ahn patent in view of U.S. Patent No. 6,301,172 to Derner *et al.* (the "Derner patent").

Claims 1, 18, 27, 36, and 45 have been amended to correct a typographical error. It will be apparent from the amendments, and the comments below, that the amendments were made independent of the cited references. None of previously mentioned amendments narrow or further limit the scope of the invention as recited by the respective claim. Generally, the amendments make explicit what is implicit in the claim, add language that is inherent in the unamended claim, or merely redefine a claim term that is previously apparent from the description in the specification. Consequently, the amendments should not be construed as being "narrowing amendments," because these amendments were not made for a substantial reason related to patentability.

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Embodiments of the present invention are directed to a digit line architecture that includes digit lines having two portions that are formed from different layers of the semiconductor structure. In one embodiment, each column of memory includes a buried digit line ("BDL") portion and a metal digit line ("MDL") portion. The BDL portions of a column of memory are located within the same memory array while the MDL portions of the column are located in different memory arrays. As a result, the digit line architecture has characteristics of both a folded digit line architecture and an open digit line architecture. In Figure 2 of the present application, a column 40 of the memory array 16 includes first and second BDL portions 42, 44 and a first MDL portion 46 of the column 40 are located in the memory array 16. A second

MDL portion 48 of the column 40, however, is located in the memory array 14. This arrangement provides a certain degree of noise immunity since the BDL portions of a column are located in the same memory array (*i.e.*, demonstrating aspects of a folded digit line architecture) and reduced digit line coupling since the MDL portions of the column are located in different memory arrays (*i.e.*, demonstrating aspects of a open digit line architecture). Moreover, the MDL portion that extends into the memory array not including the BDL portions provides capacitive balance to the MDL portion in the same memory array in which the BDL portions are located.

As described in the present application, operation of the digit line architecture is similar to conventional sensing operations. The voltage of the digit line will change from a precharge voltage based on the data state stored by the respective memory cell in response to the coupling. Following the activation of the word line, the digit lines of the accessed columns of memory are coupled through the isolation circuits to a respective sense amplifier. The sense amplifier compares the voltage of the digit line to which the memory cell is coupled and the voltage of the second digit line of the pair (which has a voltage at the precharge voltage), and amplifies the voltage difference between the two digit lines to complete the sensing operation.

For example, with reference to Figure 2, a word line 60 of a row of memory cells is activated in the memory array 10 to couple the memory cells 62-69 to the BDL portions of the active columns of memory. With respect to the memory cell 62, the memory cell 62 is coupled to the BDL portion 52 of the column 50 when the word line 60 is activated. The data state stored by the memory cell 62 will change the voltage of the digit line having the BDL portion 52 and the MDL portion 58 from the precharge voltage. The isolation circuit 36a couples the digit line having the BDL portion 54 and the MDL portion 56, and the digit line having the BDL portion 52 and the MDL portion 58 to the sense amplifier 22a for sensing. As shown in Figure 2, the BDL portions 52, 54 of the column 50 are located within the same memory array, namely, the memory array 14. However, the MDL portions of the column 50 are located in two different memory arrays, with the MDL portion 56 located in the memory array 14, and the MDL portion 58 located in the memory array 16.

In contrast, the Ahn patent describes a folded digit line architecture that couples two different columns, that is, four different digit lines to a sense amplifier. Each of the four

digit lines is coupled to approximately half as many memory cells in comparison with conventional digit line architectures. *See* col. 3, lines 10-13 and 47-49. The four digit lines coupled to each sense amplifier are formed from two different layers and are associated with a common memory array. By coupling twice as many columns of memory to a sense amplifier as conventional digit line architectures, with digit lines that are half as long, the digit line loading and current consumption is reduced. *See* col. 2, lines 14-17. The Ahn patent further describes including a "twist" in adjacent digit lines to improve overall signal-to-noise ratio. *See* col. 4, lines 18-26.

The digit lines of the two columns are coupled to a single sense amplifier and belong to the same memory cell array. *See* col. 3, lines 55-58. A set of sense amplifiers is shared between two memory arrays, with the selection of which pairs of digit lines to couple to the sense amplifier based on four signals. The four signals shown in Figure 2 of the Ahn patent are BS1, BS2, BS3, and BS4. The BS1 and BS2 signals are used to couple the columns of the memory array AR0 to the sense amplifiers 10 and the BS3 and BS4 signals are used to couple the columns of the memory array AR1 to the sense amplifiers 10. Two signals per memory array are needed to select only one of the two columns per sense amplifier during a memory cell access operation.

As previously mentioned, claims 1, 2, 4-11, 13-20, 22-29, 31-38, and 40-54 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Ahn patent.

Claim 1 is patentably distinct from the Ahn patent. Claim 1 recites a column of memory cells comprising first and second digit lines coupled to a sense amplifier, each digit line having first and second digit line portions, the first digit line portions of the first and second digit lines associated with a first memory array, the second digit line portion of the first digit line associated with the first memory array, and the second digit line portion of the second digit line associated with a second memory array. A plurality of memory cells are coupled to the first and second digit lines. The Ahn patent fails to disclose the combination of limitations recited in claim 1. For example, the Ahn patent fails to at least disclose the digit lines having two portions with one of the digit lines having one of those portions associated with a second memory array. As previously discussed, the Ahn patent is directed to a folded digit line architecture where two columns of memory are coupled to one sense amplifier. Each of the columns of memory have

two digit lines that are approximately half as long as a digit line for a conventional digit line architecture. The two columns of memory (i.e., four digit lines) are associated with one memory array and are selectively coupled to one sense amplifiers using two signals. No portion of the digit lines of a column extend into another memory array. The digit lines of the columns of memory extend through the memory array to which the columns of memory are associated, as shown in Figure 2.

For the foregoing reasons, claim 1 is patentably distinct from the Ahn patent. Claims 2-7, which depend from claim 1, are similarly patentably distinct based on their dependency from allowable base claim 1. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable.

Claims 8, 9, 18, 27, and 36 are also patentably distinct from the Ahn patent. Claims 8, 9, 18, 27, and 36 recite a combination of limitations that are not disclosed in the Ahn patent. Claims 8, 9, 18, 27, and 36 recite a combination of limitations that include a digit line architecture where a portion of a pair of digit lines extends into another memory array. As previously discussed, the Ahn patent at the very least fails to disclose digit lines having a portion that extend into another memory array. The Ahn patent describes to a folded digit line architecture where four digit lines of two columns of memory are coupled to one sense amplifier. Since each digit line is about half as long as a digit line of a conventional digit line architecture, and two different layers are used for the digit lines, the digit line architecture of the Ahn patent does not require much additional layout area. The pair of digit lines, however, does not include one digit line having a portion that extends into another memory array.

For the foregoing reasons, claims 8, 9, 18, 27, and 36 are patentably distinct from the Ahn patent. Claims 10-17, which depend from claim 9, claims 19-26, which depend from claim 18, claims 28-35, which depend from claim 27, and claims 37-49, which depend from claim 36, are similarly patentably distinct from the Ahn patent based on their dependency from a respective allowable base claim.

Claims 45 and 50 are also patentably distinct from the Ahn patent. Claim 45 recites a method for forming columns of memory cells having first and second digit lines for an array of memory cells, the method comprising forming first digit line segments to which the

memory cells are coupled of the first and second digit lines in a first memory array region, forming a second digit line segment of the first digit line in the first memory array region, and forming a second digit line segment of the second digit line extending into a second memory array region non-adjoining the first memory array region.

Claim 50 recites a method for sensing a column of memory cells for an array of memory cells having at least first and second memory sub-arrays in which the memory cells are arranged in rows and columns, the method comprising activating a row of memory of the first memory sub-array, coupling a first digit line of the column of memory cells in the first memory sub-array to a respective sense amplifier, the first digit line having a first digit line portion to which memory cells of the column are coupled and further having a second digit line portion, both digit line portions located in the first memory sub-array, coupling a second digit line of the column of memory cells in the first memory sub-array to the respective sense amplifier, the second digit line having a first digit line portion to which memory cells of the column located in the first memory sub-array and further having a second digit line portion extending into the second memory sub-array, and detecting and amplifying a voltage difference between the first and second digit lines.

The Ahn patent fails to disclose the combination of limitations recited by claims 45 and 50. For example, the Ahn patent fails to disclose forming a second digit line segment of the second digit line extending into a second memory array region non-adjoining the first memory array region. The Ahn patent further fails to disclose a method for sensing a column of memory where a second digit line has a first digit line portion to which memory cells of the column located in a first memory sub-array and further having a second digit line portion extending into a second memory sub-array. As previously discussed with respect to claims 1, 8, 9, 18, 27, and 36, the Ahn patent discloses a folded digit line architecture where two columns instead of one column are coupled to one sense amplifier. None of the pairs of digit lines of the two columns include one digit line that has one portion that extends into another memory array. The four digit lines extend into the same memory array to which the respective column of memory is associated.

For the foregoing reasons, claims 45 and 50 are patentably distinct from the Ahn patent. Claims 46-49, which depend from claim 45, and claims 51-54, which depend from claim

50, are similarly patentably distinct from the Ahn patent based on their dependency from a respective allowable base claim.

Claims 3, 4, 12, 21, 30, and 39, which have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Ahn patent in view of the Derner patent, are further patentable because the Derner patent, which has been cited by the Examiner as teaching a plurality of memory cells having a 6F semiconductor structure, fails to make up for the deficiencies of the Ahn patent, as previously discussed with respect to claims 1, 8, 9, 18, 27, and 36. That is, even if the Derner patent is taken for the teachings are characterized by the Examiner, the combination of limitations recited by claims 3, 4, 12, 21, 30, and 39 are not taught or suggested by the combined teachings of the Ahn and Derner patent.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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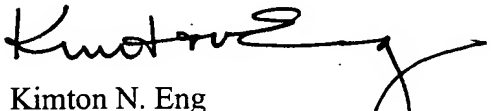

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